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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,016	02/10/2004	Dong-Soo Chang	5649-1236	9073

20792 7590 02/02/2006

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EXAMINER	
DOTY, HEATHER ANNE	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 02/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,016	CHANG, DONG-SOO	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al. (U.S. 6,632,718) in view of Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, second edition, 2000) and Wolf (*Silicon Processing for the VLSI Era*, vol. 3. first edition, 1995).

Regarding claim 1, Grider et al. teaches a method of fabricating a CMOSFET comprising forming a plurality of gate patterns on a first region (**120** in Fig. 1C) and a second region of a semiconductor substrate (**122** in Fig. 1C; Grider et al. claim 1); then forming gate spacers on both sidewalls of the gate patterns (**114** in Fig. 1C); forming a first impurity region of a first conductivity type in the first region of the semiconductor substrate (**124** in Fig. 1D; column 3, lines 12-19); then removing the gate spacers exposed at the first region (Fig. 1E; column 3, lines 20-22); then forming a second impurity region from which the gate spacers have been removed, the second impurity region having shallower depth than the first impurity region (**126** in Fig. 1E; column 3, lines 23-26); then forming a third impurity region of a second conductivity type in the second region (**134** in Fig. 1F; column 3, lines 54-58); then removing the gate spacers exposed at the second region (Fig. 1G; column 3, lines 59-61); and then forming a

fourth impurity region of the second conductivity type in the second region, the fourth impurity region having shallower depth than the third impurity region (**136** in Fig. 1G; column 3, lines 62-65), wherein the first impurity region has higher impurity concentration than the second impurity region (column 2, lines 19-27—the first and third impurity regions are source/drain implants while the second and third impurity regions are *lightly-doped* source/drain implants, which by definition have lower impurity concentrations).

Grider et al. does not teach that the fourth impurity region has impurity concentration as high as the third impurity region.

Wolf et al. teaches that in a deep submicron FET, the doping level of a source/drain extension (corresponding to the second and fourth impurity regions) can be as high as the source/drain impurity concentration (corresponding to the first and third impurity regions) ($1x10^{15}$ cm^{-2}, vol. 1, pg. 834, lines 4-7 and third full paragraph).

Although in the above-quoted section, Wolf et al. appears to teach giving the first impurity region an impurity concentration as high as the second impurity region, Wolf additionally teaches that it is beneficial in PMOS structures to have a lightly-doped LDD tip region shallower than the heavily doped p+ source/drain region to limit punchthrough (vol. 3, paragraph bridging pp. 308-309).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use the method of fabricating the CMOSFET of claim 1, as taught by Grider et al., and further fabricate the CMOSFET so that the fourth impurity region has an impurity concentration as high as the third impurity region, while leaving

the first impurity region with a higher impurity concentration than the second impurity region, as taught by Wolf et al.

The motivation at the time of the invention for giving the fourth impurity region an impurity concentration as high as the third impurity region would have been to fabricate a deep submicron FET, using ion implantation to form the source/drain extensions, as expressly taught by Wolf et al. The motivation for leaving the first impurity region with a higher impurity concentration than the second impurity region would be to limit punchthrough in the PMOS device, as expressly taught by Wolf.

Regarding claim 4, Grider et al, Wolf et al., and Wolf together teach the method of claim 1. Grider et al. further teaches that the first impurity region is formed in the first region, using the gate pattern and the gate spacers as an ion implantation mask (**124** in Fig. 1D; column 3, lines 12-19); the second impurity region is formed in the first region, using the gate pattern as an ion implantation mask (**126** in Fig. 1E; column 3, lines 23-26); the third impurity region is formed in the second region, using the gate pattern and the gate spacers as an ion implantation mask (**134** in Fig. 1F; column 3, lines 54-58); and the fourth region is formed in the second region, using the gate pattern as an ion implantation mask (**136** in Fig. 1G; column 3, lines 62-65).

Regarding claim 5, Grider et al, Wolf et al., and Wolf together teach the method of fabricating the CMOSFET of claim 1. Grider et al. further teaches that the gate spacers comprise silicon (SiGe, column 2, lines 52-61).

Regarding claim 6, Grider et al, Wolf et al., and Wolf together teach the method of fabricating the CMOSFET of claim 1. Grider et al. further teaches that removing the

gate spacers at the first and second regions is performed by isotropic etching (column 3, lines 20-22 and 59-61).

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al. (U.S. 6,632,718), Wolf et al. (*Silicon Processing for the VLSI Era*, vol. 1, second edition, 2000) and Wolf (*Silicon Processing for the VLSI Era*, vol. 3. first edition, 1995), as applied to claim 1 above, and further in view of Chen et al. (U.S. 2002/0001910).

Regarding claims 7 and 8, Grider et al., Wolf et al., and Wolf together teach the method of fabricating the CMOSFET of claims 1 (note 35 U.S.C. 103(a) rejection above), but do not teach before forming the third impurity region, forming a first HALO ion implantation to form a first HALO region, wherein the first HALO region is formed to cover sides of the first impurity region beneath the second impurity region, or after forming the fourth impurity region, performing a second HALO ion implantation to form a second HALO region, wherein the second HALO region is formed to cover sides of the third impurity region beneath the fourth impurity region.

Chen et al. teaches a method of fabricating a MOSFET that involves ion-implanting source/drain regions (**48** and **50** in Fig. 5) using spacers (**46** in Fig. 5) to mask the implantation, removing the spacers (Fig. 6), and performing a second, shallow ion implantation (**52** in Fig. 6), and then performing a HALO ion implantation (**96** in Fig. 6), using the gate pattern of the MOSFET region as an ion-implantation mask, wherein the HALO region is formed to cover the sides of the source/drain regions (Fig. 6). Chen

et al. teaches that the purpose of the HALO implantation is to inhibit the occurrence of abnormal punch-through between the source and drain (paragraphs 0035-0036).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Grider et al. and Chen et al. by fabricating MOSFET gates with spacers in two regions of a semiconductor substrate, mask one of the regions with photoresist, form deep impurity regions in the first region of the semiconductor, remove the spacers, and form shallow impurity regions in the first region of the semiconductor as taught by Grider et al., and then perform HALO implantations to cover the sides of the deep implant regions beneath the shallow implant regions using the gate pattern of the first-region MOSFET as an implantation mask, as taught by Chen et al. Grider et al. teaches that the second semiconductor region is covered in a photoresist layer, so the HALO implantation would necessarily also use that photoresist layer as a mask. It would then be obvious to continue with the method as taught by Grider et al. and mask the first semiconductor region and repeat the process in the second semiconductor region, again inserting the HALO implantation step, as taught by Chen et al. after the last shallow implantation step, since Chen does not limit this method to a particular type of MOSFET (paragraph 0035).

The motivation for doing so at the time of the invention would have been to minimize the occurrence of abnormal punch-through between the source and drain of the individual MOSFETs, as expressly taught by Chen et al.

Response to Arguments

Applicant's arguments with respect to claims 1 and 4-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

Carl Whitehead

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